second zone forming one of the source/drain zones of the transistor and the said further surface zone forming the other one of the source/drain zones of the transistor, the said first zone of the second conductivity type being situated at a shorter lateral distance from the surface zone of the first conductivity type provided in the well than the said further surface zone.

7. (Twice Amended) The semiconductor device of Claim 6, wherein the gated diode is provided on one end of the longitudinal zone and comprises the insulated gate and the highly doped second conductivity type surface zone which partly overlaps the well of the second conductivity type.

8. (Amended) The semiconductor device of Claim 7, wherein the gated diode is arranged as a MOS transistor having a further zone of the second conductivity type.

9. (Twice Amended) The semiconductor device of Claim 7, wherein the cathode of the SCR is provided along the part of the periphery of the well of the second conductivity type that is free from the gated diode.

REMARKS

Claims 1-9 are pending. By this amendment, the specification and claims 1-3 and 7-9 have been amended. Reconsideration and allowance are respectfully requested in view of the above amendments and the following remarks. No new matter is believed added.

The specification has been amended to correct a typographical error.

Claims 1-9 are rejected under 35 U.S.C. 112, first paragraph, as allegedly containing subject matter which was not described in the specification in such a way as to reasonable convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. This rejection is moot in view of the amendments to the claims.

Claims 1-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ker et al. (US 5,572,394), hereafter "Ker." This rejection is defective because Ker fails to teach or suggest each and every feature of the claims as required by 35 U.S.C. 103.

Regarding independent claim 1, Ker fails to teach or suggest, *inter alia*, the claimed first and second zones and gated diode having a gate, wherein the second zone is "aligned to this gate" and "the said second zone stretches out only along a part of the periphery of the well, the first zone is provided along at least another part of this periphery of the well which is free from the said second zone, and an anode and cathode of the SCR element in the first zone are not shielded from one another by the gated diode." These features are illustrated, for example, in FIGS. 4-6 of the present patent application. Ker does not disclose this claimed structure as clearly evidenced by the layout shown in FIG. 11 and the cross-sectional view of FIG. 11 illustrated in FIG. 9. In particular, from FIG. 11, it appears that the gates of NTLSCR1 and NTLSCR2 extend along substantially the entire length of their corresponding n-wells.

Accordingly, since Ker fails to teach or suggest each and every feature of independent claim 1 as required by 35 U.S.C. 103(a), Applicants respectively submit that claim 1 and its dependent claims are allowable.

If the Examiner believes that anything further is necessary to place the application in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney at the telephone number listed below.

Respectfully submitted,

Dated: 1/3/03

Ronald A. D'Alessandro, Jr.
Reg. No. 42,456

Hoffman, Warnick & D'Alessandro LLC
Three E-Comm Square
Albany, NY 12207
(518) 449-0044 - Telephone
(518) 449-0047 - Facsimile

DOCKET NO. PHN17-073A

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Schroeder et al.	)	Examiner: Nadav, O.
Application No.: 09/389,826	)	Art Unit: 2811
Filed: 09/03/1999	)	
For: SEMICONDUCTOR DEVICE	)	

Box Non-Fee Amendment
Commissioner for Patents
Washington D.C. 20231

SEPARATE MARKUP SHEET

In the Specification

Please amend the paragraph starting on page 5, line 13 as follows:

Fig. 4 shows a plan view of an ESD protection according to the invention having another layout compared with the previous example. Cross-sections of the device along the lines V-V and VI-VI are represented in Fig. 5, Fig. 6 respectively. The n-type well [18] 11 is arranged in the form of a longitudinal zone having two ends on the left and right-hand side of the drawing. The anode 8 is formed by a longitudinal p-type zone in the n-well 11 which well has in its center an opening at the position of which a highly doped n-type zone 12 is provided which forms a contact area for the well 11. The gated diode is solely provided on the right-hand end and comprises the insulated gate 18 and the highly doped n-type zone 17 which partly overlaps the well 11. In this example, the

gated diode is also arranged as a MOS transistor having a further n-type zone 19. The cathode of the SCR, formed by the highly doped n-type zone 14 is provided along the part of the periphery of the well 11 that is free from the gate 18 at a minor distance from the anode 8. The ratio between the two parts of the periphery may be chosen with relatively large freedom depending on the circumstances. Fig. 4 shows an embodiment in which the gated diode takes up only a relatively small part of the periphery of the SCR and thus has very little influence on the holding voltage V_h and on the current-conveying power of the SCR. At the position of the contact 20, the gate 18 is connected to the p-type substrate 10 and to the n-type cathode 14 which, together with the further zone 19, forms a coherent area. Needless to observe that, if so desired, the gate may also be connected to a junction in the circuit to another, suitable, voltage.

In the Claims

Please amend claims 1-3 and 7-9 as follows:

1. (Thrice Amended) A semiconductor device having a semiconductor body which on a surface comprises an integrated circuit containing protection means for protection against electrostatic discharge (ESD), the means being a compound element of an SCR and [at least two gated diodes] a gated diode, the protection means being provided in a surface area of a first conductivity type having a single well of a second, opposite, conductivity type,

wherein a surface zone of the first conductivity type forms a first anode and cathode area of the SCR element,

the surface area has a surface zone of the second conductivity type, further denoted as first zone, situated remote from the well and forming a second anode and cathode area of the SCR element, and

the [at least two gated diodes contain] gated diode contains a gate insulated from the surface of the semiconductor body and a highly-doped second conductivity type surface zone aligned to this gate further denoted as second zone, which aligned surface zone partly overlaps the well of the second conductivity type, characterized in that the said second zone stretches out only along a part of the periphery of the well, [whereas] the first zone is provided along at least another part of this periphery of the well which is free from the said second zone, and an anode and cathode of the SCR element in the first zone are not shielded from one another by the gated diode.

2. (Twice Amended) A semiconductor device as claimed in claim 1, characterized in that the gate of the [at least two gated diodes] gated diode substantially stretches out only along that part of the periphery of the well along which also the said second zone of the second conductivity type stretches out.

3. (Twice Amended) A semiconductor device as claimed in claim 2, characterized in that the [at least two gated diodes are] gated diode is arranged in the form of a MOS transistor which has a further surface zone of the second conductivity type, deposited in the surface area of the first conductivity type, the said second zone forming one of the source/drain zones of the transistor and the said further surface zone forming the other one of the

source/drain zones of the transistor, the said first zone of the second conductivity type being situated at a shorter lateral distance from the surface zone of the first conductivity type provided in the well than the said further surface zone.

7. (Twice Amended) The semiconductor device of Claim 6, wherein the [at least two gated diodes are] gated diode is provided on one end of the longitudinal zone and comprises the insulated gate and the highly doped second conductivity type surface zone which partly overlaps the well of the second conductivity type.

8. (Amended) The semiconductor device of Claim 7, wherein the [at least two gated diodes are] gated diode is arranged as a MOS transistor having a further zone of the second conductivity type.

9. (Twice Amended) The semiconductor device of Claim 7, wherein the cathode of the SCR is provided along the part of the periphery of the well of the second conductivity type that is free from the [at least two gated diodes] gated diode.